

SUPERCOMPUTER "FUGAKU" DEVELOPMENT

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FUJITSU LIMITED

Supercomputer “Fugaku”, Formerly Known as Post-K

- “Fugaku” is named after Mt. Fuji

- Highest mountain in Japan

- Very broad gradual slopes






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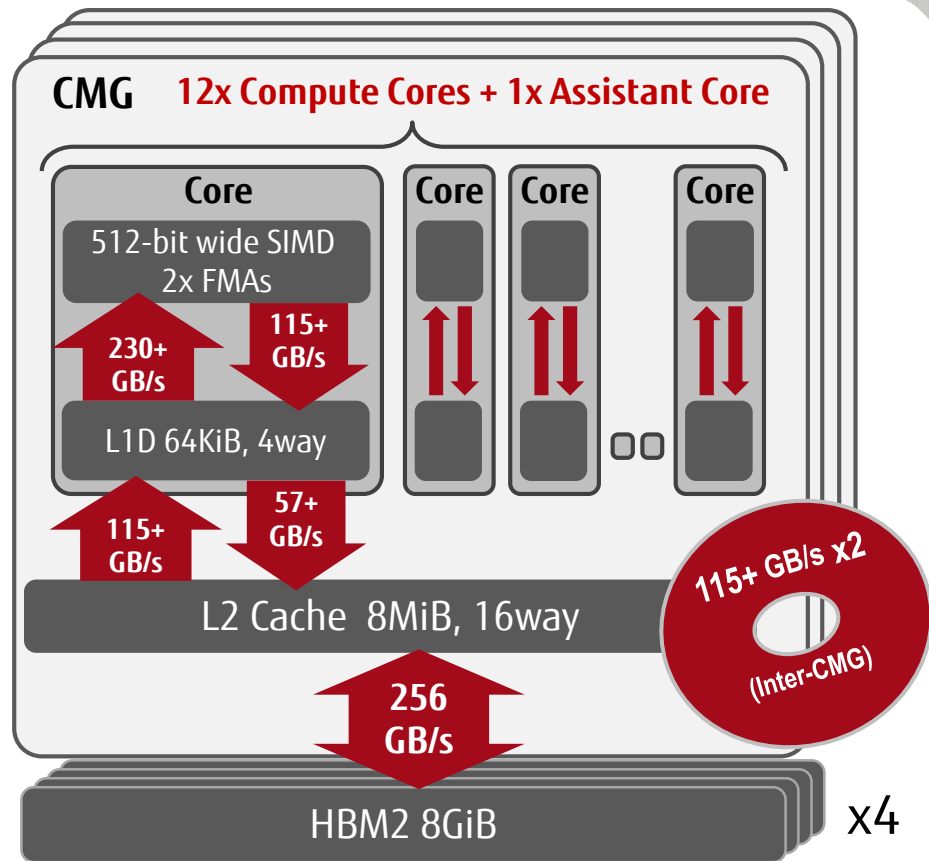


Focus	Approach
 Application performance	Co-design w/ application developers and Fujitsu-designed CPU core w/ high memory bandwidth utilizing HBM2
 Power efficiency	Leading-edge Si-technology, Fujitsu's proven low power & high performance logic design, and power-controlling knobs
 Usability	Arm®v8-A ISA with Scalable Vector Extension (“SVE”), and Arm standard Linux

Fujitsu-designed CPU Core w/ High Memory Bandwidth

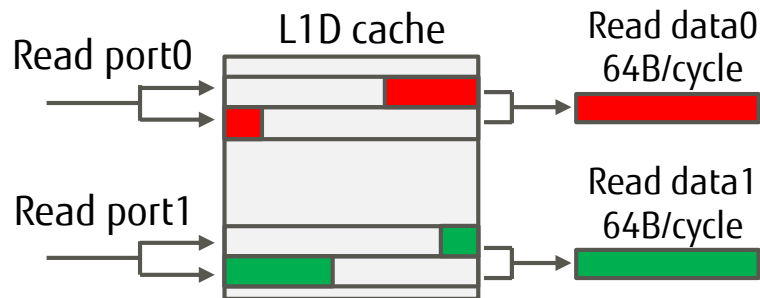
- A64FX out-of-order controls in cores, caches, and memories achieve superior throughput

BW and calc. perf.	A64FX	B/F
DP floating perf. (TFlops)	2.7+	-
L1 data cache (TB/s)	11+	4
L2 cache (TB/s)	3.6+	1.3
Memory BW (GB/s)	1024	0.37

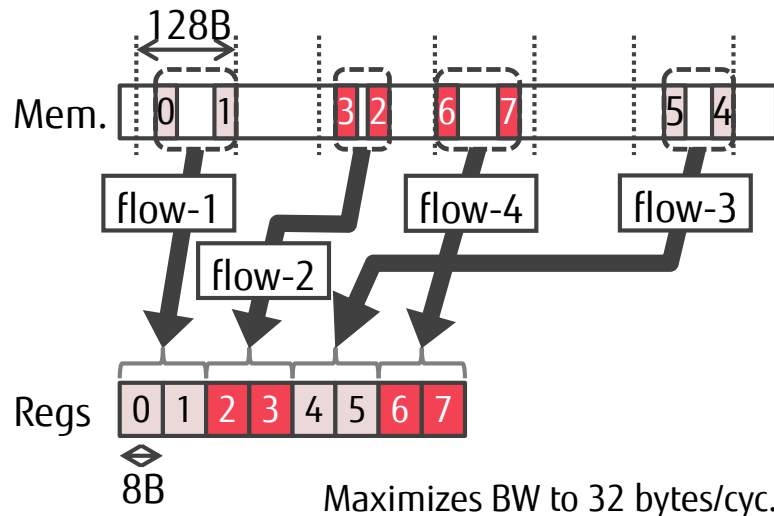


A64FX Optimized Load Efficiency for Apps Performance

- 128 bytes/cycle sustained bandwidth even for unaligned SIMD load



- “Combined Gather” doubles gather (indirect) load’s data throughput, when target elements are within a “128-byte aligned block” for a pair of two regs, even & odd

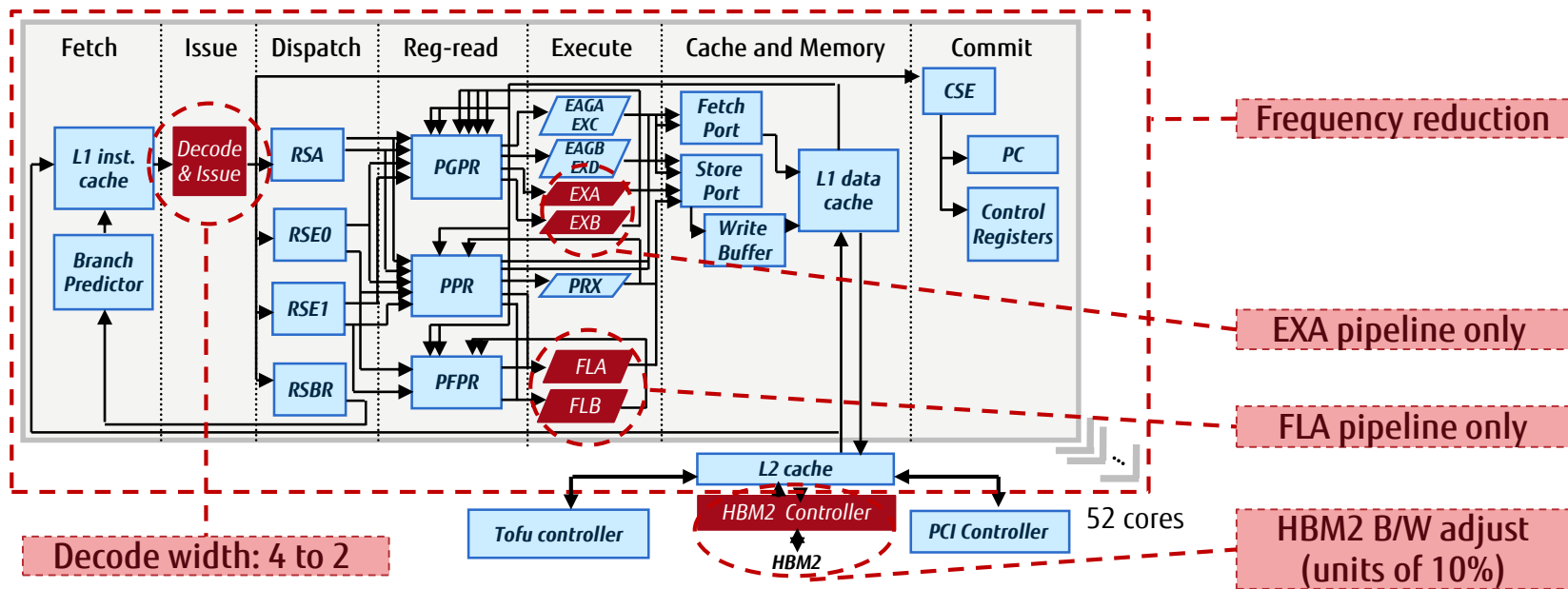


Suggested through Co-design work w/ app teams

Maximizes BW to 32 bytes/cyc.

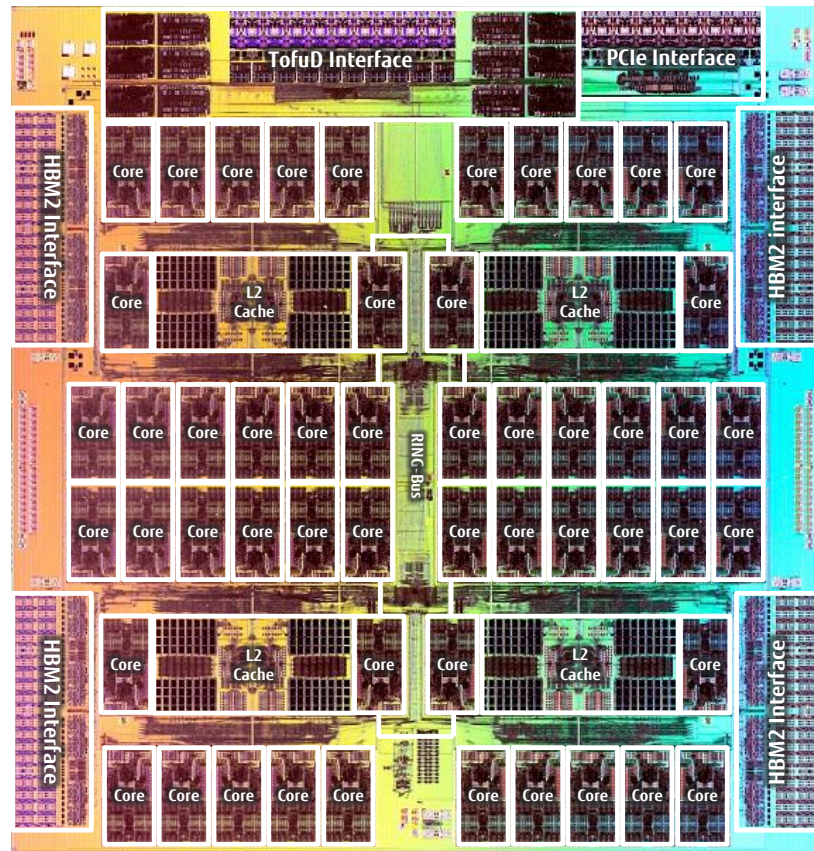
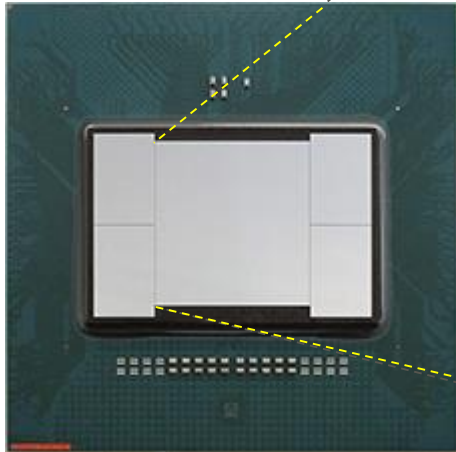
A64FX Power Knobs to Reduce Power Consumption

- “Power knob” limits units’ activities via user APIs
- Performance/Watt can be optimized by utilizing Power knobs



A64FX Leading-edge Si-technology

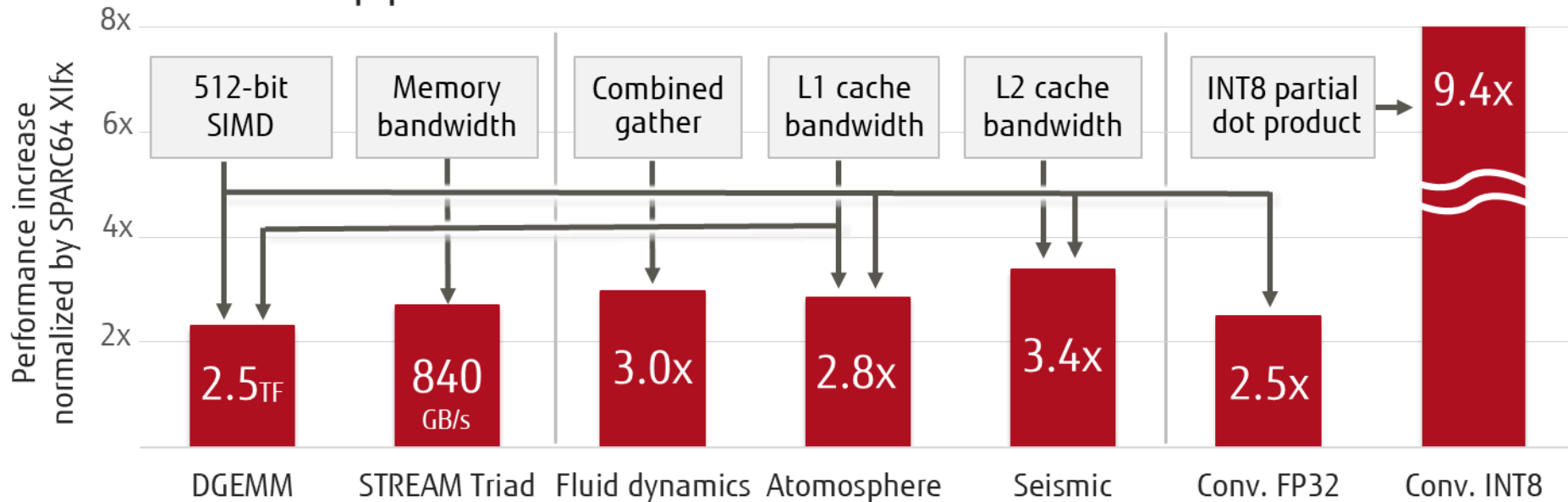
- TSMC 7nm FinFET & CoWoS
 - Broadcom SerDes, HBM I/O, and SRAMs
 - 87.86 billion transistors
 - 594 signal pins



"Fugaku" CPU Performance Evaluation (1/3)

- Over 2.5x faster in HPC & AI benchmarks than SPARC64 XIfx

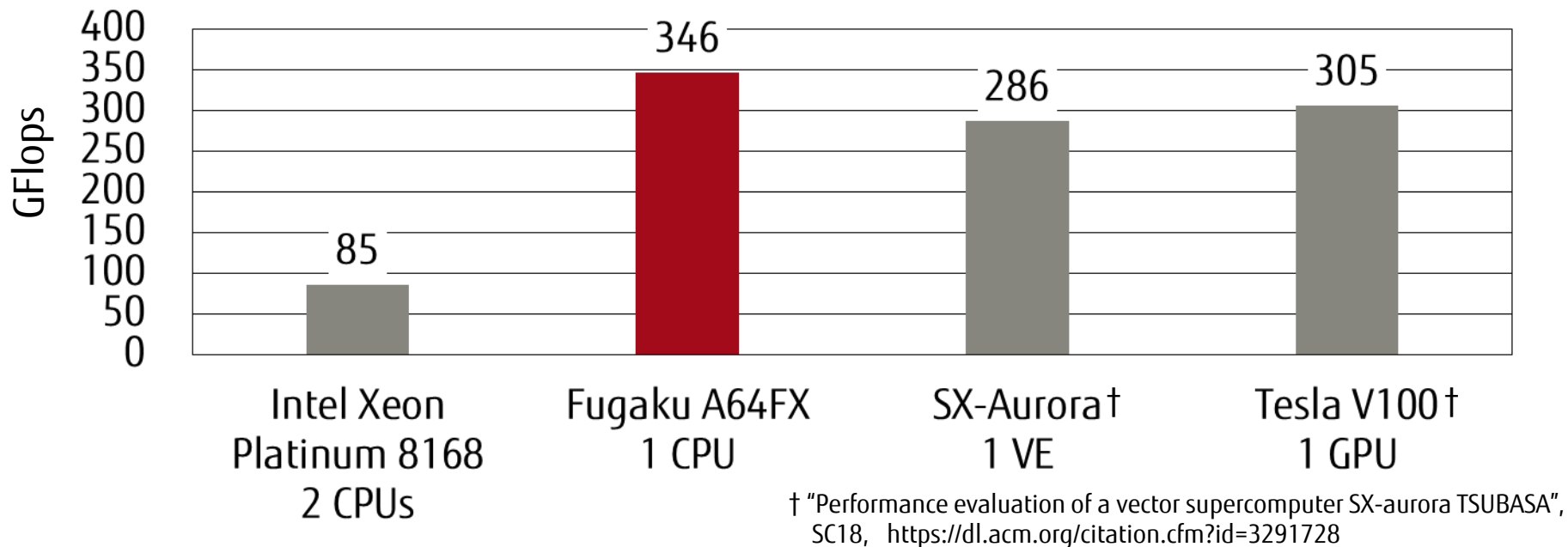
A64FX chip performance measurements & architectural contributions



"Fugaku" CPU Performance Evaluation (2/3)

■ Himeno Benchmark (Fortran90)

■ Stencil calculation to solve Poisson's equation by Jacobi method

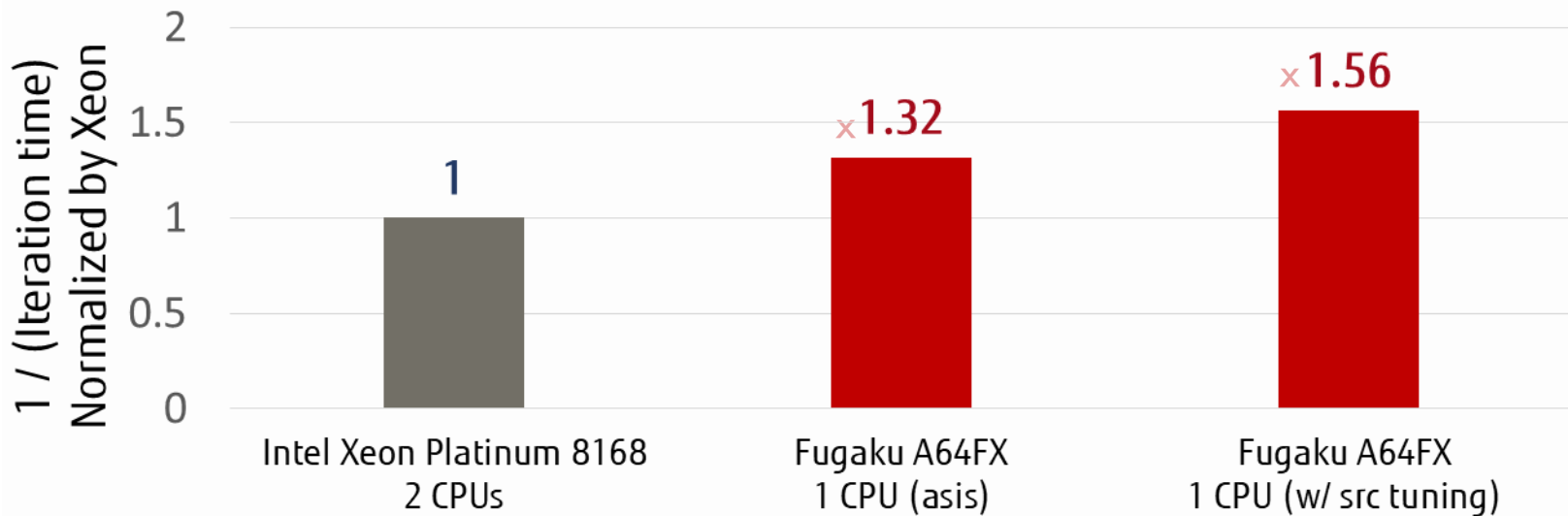


"Fugaku" CPU Performance Evaluation (3/3)

■ WRF: Weather Research and Forecasting model

- Vectorizing loops including IF-constructs is key optimization
- Source code tuning using directives promotes compiler optimizations

WRF v3.8.1 (48-hour, 12km, CONUS) on 48 cores



OSS Application Porting @ Arm HPC Users Group

(<http://arm-hpc.gitlab.io/>)

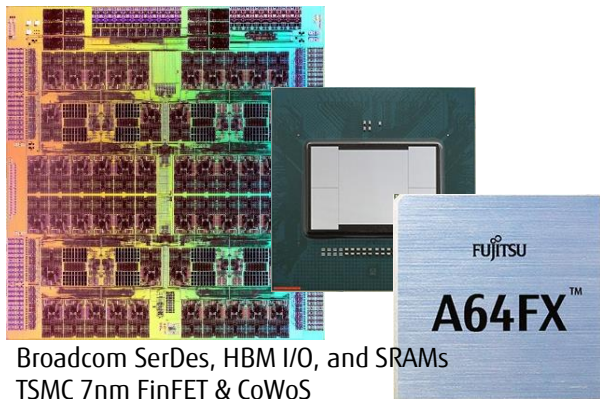
Application	Lang.	GCC	LLVM	Arm	Fujitsu
LAMMPS	C++	Modified	Modified	Modified	Modified
GROMACS	C	Modified	Modified	Modified	Modified
GAMESS*	Fortran	Modified	Modified	Modified	Modified
OpenFOAM	C++	Modified	Modified	Modified	Modified
Siesta*	Fortran	Ok in as is	Issues found	Issues found	Modified
NAMD	C++	Modified	Modified	Modified	Modified
WRF	Fortran	Modified	Modified	Modified	Modified
Quantum ESPRESSO	Fortran	Ok in as is	Ok in as is	Ok in as is	Modified
NWChem	Fortran	Ok in as is	Modified	Modified	Modified
ABINIT	Fortran	Modified	Modified	Modified	Modified
CP2K	Fortran	Ok in as is	Issues found	Issues found	Modified
NEST*	C++	Ok in as is	Modified	Modified	Modified
USQCD (MILC)	C	Ok in as is	Modified	Modified	Modified
BLAST*	C++	Ok in as is	Modified	Modified	Modified

Summary: “Fugaku” and Fujitsu Commercial Units



- “Fugaku” is designed and runs applications at the highest level performance to be worthy of the name
- Arm HPC ecosystem and expanding apps portfolio are likened to the broad gradual slopes of Mt. Fuji

Fujitsu designed 48-core CPU

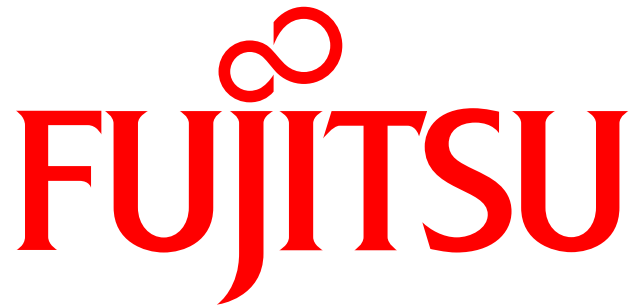


Broadcom SerDes, HBM I/O, and SRAMs
TSMC 7nm FinFET & CoWoS

- Fujitsu began production of “Fugaku”, also advances productization of commercial units based on the supercomputer technology

Image of commercial unit from Fujitsu





shaping tomorrow with you